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PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION METHODS AND SEMICONDUCTOR PROCESSING METHODS OF FORMING LAYERS AND SHALLOW TRENCH ISOLATION REGIONS

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PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION METHODS AND SEMICONDUCTOR PROCESSING METHODS OF FORMING LAYERS AND SHALLOW TRENCH ISOLATION REGIONS

TECHNICAL FIELD

This invention relates to plasma enhanced chemical vapor deposition methods, to semiconductor processing methods of forming layers and shallow trench isolation regions, and to plasma enhanced chemical vapor deposition methods of forming SiO_2 comprising layers.

BACKGROUND OF THE INVENTION

The processing of a semiconductor substrate to form integrated circuitry involves forming numerous layers over the substrate. Many of the layers are formed by a chemical vapor deposition (CVD) process involving placing the substrate within an elevated temperature environment provided by a reactor and providing reactant gases within the reactor. Successive layers are provided by successive CVD processes. However, characteristic temperatures of a typical CVD process may not be conducive to layers already formed over the substrate. For example, subsequent CVD processing of a substrate having an aluminum layer will cause unacceptable alloying of the aluminum into the substrate. Accordingly, plasma enhanced chemical vapor deposition (PECVD) techniques were developed that include forming a plasma within a reactor and using the energy of the plasma in an environment with a lower

temperature to form the layers. Consequently, the PECVD process is more conducive to temperature sensitive layers than a non-plasma CVD process.

PECVD systems typically feature a parallel plate chamber within a reactor operated at a low pressure. A plasma source is used to generate a plasma field within the reactor, for example, radio-frequency-induced glow discharge, high density inductively coupled plasma, or other plasma sources within an environment of reactant gases provided within the reactor. Such PECVD systems are physically similar to plasma etch systems, and therefore, are capable of using the plasma field for etching a semiconductor substrate layer during the deposition processing.

One CVD and/or PECVD process forms shallow trench isolation regions within a substrate. A substrate having trench openings formed therein is provided within a reactor to form layers over the trenches thereby filling the same. However, as the semiconductor industry strives to increase the density of components per unit area of semiconductor substrate, the width of the trench openings continues to shrink such that depositing the layer within the trenches can be problematic.

Figs. 1-2 illustrate the problem. A semiconductor substrate is generally indicated by numeral 10 and comprises a bulk substrate 12 having trenches 14 formed therein. The substrate is provided in a reactor (not shown) and a layer of insulative material 16 is deposited over the substrate 12 within the trenches 14. As layer 16 is deposited,

the insulative material begins to build up over corners 17 of the trenches 14 forming facets or bread-loafing regions 18.

Referring to Fig. 2, as layer 16 continues to be deposited, the bread-loafing regions 18 begin to occlude the trench openings and form voids 20 within the portion of layer 16 that progresses into the trenches 14. These voids 20 can be detrimental to the performance of the isolation regions.

To overcome this problem, inductively coupled plasma reactors can be used with a bias being placed upon the substrate during deposition. The bias attracts ions in the plasma to bombard the layer 16 effectively producing a simultaneous deposition to sputter etching aspect of processing layer 16. The purpose and result of the sputter etching is to remove the bread-loafing regions 18 during deposition of layer 16, i.e., forming the bread-loafing regions 18, removing at least some of the bread-loafing regions 18, forming the bread-loafing regions 18 and continuing the process until the trenches 14 are filled. The deposition to sputter etching aspect establishes a deposition to sputter etching ratio (also referred to as deposition to etch ratio and/or D:S ratio). An exemplary D/S ratio comprises a constant 6:1. This process can improve the deposition of layer 16 within the trenches 14.

However, such processing is not without its own drawbacks. Fig. 3 illustrates a problem (like numerals from the previously described embodiment are employed where appropriate with the difference being

indicated with a suffix (b) or with different numerals). Consider corner sections 17 of substrate 12. The etching portion of the processing can cause corner sections 17 to be etched away from substrate 12 thereby changing the profile of trenches 14. Changing the profile of trenches 14 can detrimentally affect the performance of the isolation regions. Additionally, removed material from corners 17, designated with numeral 24, can settle within the trenches 14 inside layer 16. Since the removed material 24 is routinely not an insulative material as is characteristically used for isolation regions, the performance of the isolation regions is typically detrimentally affected.

SUMMARY OF THE INVENTION

In accordance with an aspect of the invention, a substrate is placed within a plasma enhanced chemical vapor deposition reactor. A plurality of reactant gases are provided within the reactor proximate the substrate under high density plasma conditions effective to form a layer on the substrate. The conditions result in etching portions of the layer during its formation and thereby include a deposition to etch ratio of forming the layer. During the forming, the conditions are changed to change the deposition to etch ratio.

In another aspect of the invention, the invention includes a semiconductor processing method of forming shallow trench isolation regions within a semiconductive substrate. Isolation trenches are formed

within the semiconductive substrate. The substrate is provided within a plasma enhanced chemical vapor deposition reactor. A silane containing gas, an oxygen containing gas and an inert gas are injected into the reactor under high density plasma conditions effective to form a predominate SiO_2 comprising layer on the substrate to overfill the trenches. The conditions result in etching of portions of the layer during its formation and thereby includes a deposition to etch ratio of the forming SiO_2 comprising layer. During the forming, the conditions are changed to change the deposition to etch ratio.

In yet another aspect of the invention, a substrate is placed within a plasma enhanced chemical vapor deposition reactor. A plurality of reactant gases are provided within the reactor proximate the substrate under plasma conditions. The plasma conditions are effective to form a substantially homogeneous layer of material on the substrate. While continuing to form the layer, a flow of at least one of the reactant gases is reduced during at least some of the forming.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a first embodiment of a fragmentary sectional view of a prior art semiconductor substrate discussed in the "background" section above.

Fig. 2 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown in Fig. 1.

Fig. 3 is a second embodiment of a fragmentary sectional view of a prior art semiconductor substrate discussed in the "background" section above.

Fig. 4 is a fragmentary sectional view of a semiconductor substrate at one processing step in accordance with an embodiment of the invention.

Fig. 5 is a view of the Fig. 4 substrate fragment at a processing step subsequent to that shown in Fig. 4.

Fig. 6 is a view of the Fig. 4 substrate fragment at a processing step subsequent to that shown in Fig. 5.

Fig. 7 is a graphical representation of an aspect of the processing in accordance with one embodiment of the invention.

Fig. 8 is a graphical representation of an aspect of the processing in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to

mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

With reference to Figs. 4-7, an embodiment of the method of the present invention is illustrated. This embodiment encompasses a semiconductor processing method, particularly a plasma enhanced chemical vapor deposition method of forming shallow trench isolation regions within a semiconductor substrate. Referring to Fig. 4, a semiconductor substrate 42 in process is indicated generally by reference numeral 40. An exemplary semiconductor substrate 42 comprises bulk substrate material, for example, monocrystalline silicon. Isolation trenches 44 are formed within the semiconductor substrate 42 by etching methods known in the industry, and include corners 48. The substrate 42 is provided within a plasma enhanced chemical vapor deposition reactor (not shown). An exemplary reactor comprises an inductively coupled plasma reactor capable of producing a high density plasma. In the context of this document, "high density" refers to a plasma having at least 10^9 ions/cm^3 plasma density.

A plurality of reactant gases are provided within the reactor proximate the substrate 42 under plasma conditions, most preferably high density plasma conditions, effective to form a layer 46 on the substrate 42 and within trenches 44. An exemplary layer 46 comprises an electrically insulative material, for example, silicon dioxide. Exemplary reactant gases comprise a silane containing gas, an oxygen containing gas and an inert gas, for example, argon. An exemplary environment within the reactor includes a pressure preferably ranging from 0.1 mTorr to 50 mTorr, more preferably less than 5 mTorr, and a temperature of about 650°C. Exemplary flow rates of the reactant gases into the reactor comprise ranges of: argon at 0-300 sccm, oxygen at 100-300 sccm and silane at 20-200 sccm. The preferred high density plasma conditions result in etching of portions of the layer 46 during its formation and thereby include a deposition to etch ratio of the forming layer 46. An exemplary preferred initial D/S ratio of forming layer 46 is at least 7:1. This high deposition rate relative to the sputter etching rate is intended to keep outer corners 48 of the trenches covered by enough of forming layer 46 to protect such corners from being removed from the sputter etching action.

Referring to Fig. 5, deposition continues with the high density plasma conditions being changed during the forming to change the deposition to etch ratio. Most preferably, the deposition to etch ratio is decreased. Regardless, processing preferably continues to completely

fill trenches 44, as shown in Fig. 6. Preferably, layer 46 as formed is substantially homogeneous throughout.

Changing of the conditions during the forming to change the deposition to etch ratio might occur by a number of manners. Such manners might include maintaining some parameters constant while changing one or more other parameters or changing a plurality of the operating parameters during the formation regardless. By way of example only, changing of the conditions might comprise changing a flow rate of at least one reactant gas to the reactor during formation, and/or changing at least one power setting during formation such as bias power on the substrate. Further, the changing conditions might comprise maintaining constant power settings while changing a flow rate of at least one reactant gas into the reactor during formation.

In one aspect, the invention contemplates providing conditions which begin with an environment providing a large deposition rate relative to an etch rate, thereafter decreasing the ratio, and thereafter increasing the ratio. Such provides but one example where the changing of the conditions reduces the deposition to etch ratio at least once during formation. Preferably, the deposition starts with substantially no etching during initial formation.

In one aspect of the invention, the invention contemplates changing the conditions during the forming to continuously vary the deposition to etch ratio throughout at least a majority of the forming. In one

preferred implementation, changing the condition comprises continuously increasing the deposition to etch ratio at some point after a majority of the layer has been formed.

In the trench-filling example of forming SiO_2 under high density plasma conditions using a silane containing gas, an oxygen containing gas, and an inert gas, one aspect of the invention contemplates reducing a flow of at least one of the silane containing gas and the oxygen containing gas, or both, during the forming and continuing forming the layer. Such preferably has the effect of decreasing the deposition to etch ratio until such time as one or more of the flows might be increased. For example where the reactant gas silane is varied in such example, an exemplary high flow rate would be from about 60 sccm to about 150 sccm, with an exemplary low flow rate for silane being from about 20 sccm to about 60 sccm.

Figs. 7-8 together graphically represent but one example embodiment of the present invention where silane flow is varied during formation. The process begins with an environment providing a large silane flow rate which corresponds, referring to Fig. 8, to providing a large deposition rate relative an etch rate. The deposition can start with substantially no etching of the layer during its initial formation. After this beginning, the silane flow rate is decreased which corresponds to decreasing the ratio. (i.e., at some point in time after the deposition begins, the etching increases relative to the deposition.) At some point

in the example, the silane flow is increased, corresponding to an increase in the ratio, perhaps to a point which substantially eliminates etching while continuing the deposition. The illustrated example depicts a substantially continuous and parabolic profile, although any other profile is contemplated, such as by way of example, linearly, exponentially and logarithmically.

The invention was initially motivated and considered in the context of high density plasma deposition involving an etching aspect during the depositing. However, the invention also contemplates plasma enhanced chemical vapor depositing by placing a substrate within a plasma enhanced chemical vapor deposition reactor which may or may not be a high density plasma reactor, and may or may not be operated under high density plasma conditions. A plurality of reactant gases are then provided within the reactor proximate the substrate under plasma conditions effective to form a substantially homogeneous layer of material on the substrate. At some point in the process, a flow of at least one of the reactant gases is reduced during at least some of the forming and the layer is continued to be formed.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into

effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.